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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/612,129
Filing Date: July 02, 2003
Appellant(s): YEW ET AL.

W. Daniel Swayze, Jr.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/3/05.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The Brief states that there are no related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct. However, independent claim 3 is not an appealed claim and it should not be in the appealed claim appendix because independent claim 3 has already been allowed in the Office Action mailed on 8/6/2004.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Grounds of Rejection to be reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal contained in the brief is correct.

(7) Claims Appealed

A substantially correct copy of appealed claims 1-2, and 4-15 appears on pages 7-9 of the Appendix to the appellant's brief. The minor errors are as follows: independent claim 3 is not an appealed claim, it has already been allowed in the Office Action mailed on 8/6/2004.

(8) Prior Art of Record

U.S. 6,013,946	LEE et al.	01-2000
U.S. 5,300,812	LUPINSKI et al.	04-1994
J.P. 06-629454	HIROSHI, NAGAYAMA (including English translation)	02-1994

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4, and 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US. 6,013,946) in view of Lupinski et al (US. 5,300,812).

Regarding claims 1-2, 4 and 5, Lee (Fig. 3) discloses a semiconductor device comprising: an integrated circuit semiconductor chip 130 having an active and a passive surface, the active surface including a protective adhesive layer 142, and at least one bonding pad 131; an electrically insulating substrate 120a having first and second surfaces; a plurality of electrically conductive routing strips 121 (not shown in Fig. 3, see Fig. 5) integral with the substrate; a plurality of contact pads 122 disposed on the first surface of the substrate, at least one of the contact pads electrically connected with at least one of the routing strips 121 (also see Fig. 5); the second surface of the substrate

120a being directly attached to the protective adhesive layer 142; and bonding wires 150 electrically connecting the at least one bonding pad 131 to at least one of the contact pads 122.

Lee does not disclose that the protective adhesive layer 142 is a protective polymer having been preactivated.

However, Lupinski teaches the forming of an active surface and a passive surface, the active surface including a protective polymer layer 40 (column 6, lines 47-49) and at least one one bonding pad 31, the protective polymer layer 40 being preactivated to impart adhesiveness by preheated to 260 degrees C at pressure of 55 psi in a vacuum chamber for providing void free adhesive bonding (column 7, lines 3-35); and the forming of the surface of the electrically insulating substrate 50 directly on the preactivated polymer layer 40.. Accordingly, it would have been obvious to form the protective adhesive layer 142 of Lee with a polymer being preactivated, because as taught by Lupinski, such preactivated protective adhesive layer would provide void free adhesive bonding (column 2, lines 9-16 and column 7, lines 30-35).

Regarding claims 9-13, Lee's Fig. 3 further discloses: the bonding pad 131 disposed at the centerline of the chip 130; the substrate having an opening 123 and the contact pads disposed along the opening; the encapsulating material 161 covering the bonding wires 150 and the bonding pads 131 and the contact pads; and at least one solder ball 170 located on the assembly pads 122 and connected with one of the routing strips 121 (see Fig. 10).

Regarding claims 7-8, Lee further discloses the conventional device having bonding pad 52 disposed at the periphery of the chip 51 and the contact pads 54 disposed around the periphery of the substrate 53 (see Fig. 1).

Regarding claim 14, Lee does not disclose that the chip 130 and the substrate 120a have substantially the same outlines. However, it would have been obvious to form the chip 130 and the substrate 120a having the same outlines because changing in size/proportion of parts of an invention involves routine skill in the art. It has been held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. *In Gardner v. TEC Systems, Inc.*, 725 F. 2d 1338, 220 USPQ 777 (fed. Cir. 1984), *Cert. Denied*, 469 U.S. 830, 225 USPQ 232 (1984).

3. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al and Lupinski et al as applied to claim 1 above, and further in view of Hiroshi (JP. 06-029454).

Neither Lee nor Lupinski disclose a metal layer disposed on the substrate and between the substrate and the chip as claimed.

However, Hiroshi (Fig. 3) teaches the forming of a metal layer 2 on a second surface of a substrate 5 and attaching the second surface of the substrate 5 to a protective adhesive layer 4 on the chip 1. Accordingly, it would have been obvious to modify the above combination device by forming a metal layer with the structure as set

forth above, because as taught by Hiroshi, such modification would reduce the distorted stress from a lead layer (see translation, par. [0013]).

As to the grounds of rejection under section 103(a), the method for depositing the metal layer on the substrate **prior** to attaching the substrate to the adhesive layer on the chip, is an intermediate process step that does not affect the structure of the final device. See MPEP 2113 which discussed the handling of "product by process" claims and recommends the alternative (102/103) grounds of rejection.

Therefore, the process limitations recited in a "product by process" claim would not carry patentable weight in a claim drawn to structure because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

(10) Response to Argument

ISSUE NO. 1: CLAIMS 1-2, 4 AND 7-15 ARE REJECTED UNDER 35 U.S.C. 103(a) AS BEING UNPATENTABLE OVER LEE ET AL IN VIEW OF LUPINSKI ET AL.

A) Appellants argue that it would not be obvious to combine Lee with Lupinski because Lee does not suggest "the plurality of contact pads disposed on the first surface of the substrate and a second surface of the substrate being directly attached to the preactivated polymer level" (page 4 of Brief).

It should be noted that the rejection of the invention as claimed is not based on anticipation, but rather, is based on obviousness. Thus, Appellant's arguments are arguments against the references individually but, clearly, these are not proper arguments where references are applied in combination. *In re Keller*, 642 F. 2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). The examiner relied on the combined teaching

of Lee and Lupinski. Lee is relied on for teaching a plurality of contact pads 122 disposed on the first surface of the insulating substrate 120 and the second surface of the insulating substrate 120 being directly attached to the protective adhesive layer 142 (see Fig. 3), but Lee is not relied on for teaching the protective adhesive layer 142 being a protective polymer having been preactivated. Lupinski is relied on for showing that it was known to attach the active surface of a semiconductor chip 30 to an insulating substrate 50 by a preactivated polymer layer 40 for providing void free adhesive bonding (column 2, lines 9-16), the preactivated polymer layer 40 is preactivated to impart adhesiveness and to provide void free adhesive bonding by preheated to 260 degrees C at pressure of 55 psi in a vacuum chamber (column 7, lines 3-35). Therefore, it would have been obvious to combine the references as suggested because Lupinsky clearly suggests the motivation to combine. The examiner thus regards Appellants' assertions as constituting evidence that Appellants have failed to consider as a whole the prior art teachings disclosed by the combining of the references.

4. B) Appellants also argue that it would not be obvious to combine Lee with Lupinski because Lupinski does not suggest "a plurality of contact pads disposed on the first surface of the substrate and the second surface of the substrate being directly attached to the preactivated polymer level" (page 4 of Brief).

Again, It should be noted that the rejection of the invention as claimed is not based on anticipation, but rather, is based on obviousness. Therefore, Appellants' arguments above have no immediate apparent relevance to the issues presented by the

rejection since Appellants cannot show nonobviousness by attacking references individually where the rejection is based upon a combination of references. *In re Young*, 403 F.2d 754, 757, 159 USPQ 725, 728 (CCPA 1968). The examiner relies on the combined teachings of Lee and Lupinski. Lupinski is not relied on for teaching a plurality of contact pads disposed on the first surface of the substrate and the second surface of the substrate being directly attached to the adhesive layer. Lee clearly discloses a plurality of contact pads 122 disposed on the first surface of the insulating substrate 120 and the second surface of the insulating substrate 120 being directly attached to the adhesive layer 142 (see Fig. 3). Lupinski is relied on for showing that it was known to attach the active surface of a semiconductor chip 30 to an insulating substrate 50 by a preactivated polymer layer 40 for providing void free adhesive bonding (column 2, lines 9-16), the preactivated polymer layer 40 is preactivated to impart adhesiveness and to provide void free adhesive bonding by preheated to 260 degrees C at pressure of 55 psi in a vacuum chamber (column 7, lines 3-35). Therefore, it would have been obvious to combine the references as suggested because Lupinski clearly suggest the motivation to combine. The examiner thus regards Appellant's assertions as constituting evidence those Appellants have failed to consider as a whole the prior art teachings disclosed by the combining of the references.

Appellants further argue that "Lupinski does not disclose a preactive layer being used with a insulating substrate that bears a relationship to contact pads" (page 5 of Brief).

This argument is not persuasive because in contrary to Appellants' assertions, both Lee and Lupinski clearly disclose the above feature. Specifically, Lupinski (see Figure) clearly discloses a preactive layer 40 being used with an insulating substrate 50 that bears a relationship to contact pads 31, and Lee (Fig. 3) clearly discloses a protective adhesive layer 142 being used with an insulating substrate 120 that bears a relationship to contact pads 122/cond pads 131.

ISSUE NO. 2: CLAIMS 5-6 ARE REJECTED UNDER 35 U.S.C. 103 (a) AS BEING UNPATENTABLE OVER LEE ET AL AND LUPINSKI ET AL AND FURTHER IN VIEW OF HIROSHI.

Appellants argue that Hiroshi does not disclose the forming of a metal layer on a protective adhesive layer and it would not obvious to combine Hiroshi with the other applied references (page 5 of Brief).

Appellants' arguments are not persuasive because Hiroshi (Fig. 3) clearly teaches the forming of a metal layer 2 on a protective adhesive layer 4 and having a semiconductor chip 5 attaching on the metal layer 2 for reducing the distorted stress from a metal lead layer. Therefore, it would have been obvious to combine the references as suggested because Hiroshi clearly suggests the motivation of reducing the distorted stress from a metal lead layer (see translation, par. [0013]) by forming a metal layer on a protective adhesive layer and between the insulating substrate and the chip.

Appellants further argue that "the Examiner has used impermissible hindsight in order to reject the Applicant's claims" (page 5 of Brief).

This argument is not persuasive because it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to combine the references as suggested because each of the references clearly teaches the motivation to combine them. Specifically, Lupinski clearly teaches the motivation of providing void free adhesive bonding for improving adhesiveness by attaching the active surface of the semiconductor chip 30 to an insulating substrate 50 by a preactivated polymer layer 40 (column 7, lines 3-35), and Hiroshi (Fig. 3) clearly teaches the motivation of reducing the distorted stress from a metal lead layer (see translation, par. [0013]) by forming a metal layer on a protective adhesive layer 4 and between the insulating substrate 5 and the chip 1. The examiner respectfully submit

that Appellants have failed to provide the reasons to support that one of ordinary skill in the art would not combine the references as proposed by the examiner even though each of the applied references clearly suggests the motivation for combining them.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

PC
April 18, 2005

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